

**ABSTRACT OF THE DISCLOSURE**

A method of efficiently designing, implementing, and verifying programmed PLDs that includes translating simulation test vectors that are generated by design automation software into device level test vectors. Each of the device level test vectors is substantially identical to one of the simulation test vectors and is readable by automatic testers. Thus, the operation of programmed PLDs can be thoroughly and efficiently verified at the device level using the same test stimuli as a simulation test model.

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